Uncertainty Quantification for Robust Topology Optimization of Power Transistor Devices

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In this paper we focus on incorporating a stochastic collocation method (SCM) into a topology optimization for a power semiconductor device with both material and geometrical uncertainties. Such geometrical and material variations, which result predominantly from lithography proximity and process imperfections, have a direct impact on its yield and performance. This results in a stochastic direct problem and in consequence, affects the formulation of an optimization problem. Specifically, we deal with the robust optimization of a power transistor in order to minimize the current density overshoots, since the change of the shape and topology of a device layout is the proven technique for the reduction of a hotspot area. The gradient of a cost functional is evaluated using the sensitivity equation and the adjoint variable method. In simulations, we apply the level set method with a distribution additionally modified by the topological derivative, for the representation of the interface. Finally, we show the results of the robust optimization for the power transistor device, which is an example of a relevant problem in nanoelectronics, and also used widely in the automotive industry.

***Index Terms*—uncertainty quantification (UQ), robustness, topology, design optimization, nanoelectronics, power transistors.**

I. Introduction

The power semiconductor devices play a key role in efficiently exploiting resources and energy in power electronics with respect to both an energy harvesting and distribution as well as in applications for automotive industry. In fact, due to the proximity effect in lithography and several process variations, the physical domain of power devices made of several thousands of parallel channel devices, cannot be determined precisely. In particular, the imperfections in manufacturing processes related primarily to sub-wavelength lithography, lens aberration, and chemical-mechanical polishing belong to the most important variation issues, since they directly influence both the yield and performance [9]. In consequence, they determine also the acceptability, reliability and profitability of power electronic systems, which depend mainly on variation tolerances, e.g., [5]. This, in turn, is especially important in automotive applications that require the handling of electro-thermal operational constraints to the design of both components and systems. In this context, the localized imperfections of the die inside may result in the formation of a 'hot spot' (see Fig.4) that rapidly heats and leads to the destruction of a power device, e.g., [1, 7].

The problem of a thermal instability has been known to the automotive industry since the year 1997 when the very fast switching MOSFET devices were introduced onto the market [7]. This phenomenon, which is a main reason for the reduction of the safe operating area, results from a temperature instability mechanism induced by an uneven distribution in drain current as a side effect of the progressive die size and the process scaling down [1]. However, the positive temperature coefficient in a wide range of drain currents, which causes a kind of second breakdown phenomenon, is related to the geometrical and physical parameters of a power device [1, 2]. From this point of view, it is possible to reduce a thermal instability by optimizing the geometry within the device layout while taking both the conductive power losses and robustness into account. Therefore, in this work we apply the SCM [8] with the Polynomial Chaos (PC) for the assessment of the reliability and robustness of a design w.r.t. uncertain parameters from manufacturability, e.g., tolerances variations, described by random variables. This solution allows for the efficient calculation of statistical moments and additionally yields directly a response surface model, which can be easily incorporated in a robust topology optimization, e.g., [6].

A novelty of this paper is to incorporate the SCM into the Level Set Method (LSM) in order to eliminate hot-spot phenomena while taking the geometrical and material variations into account. The latter is an important requirement in real engineering applications where designers ought to consider some manufacture tolerances during the optimization process.

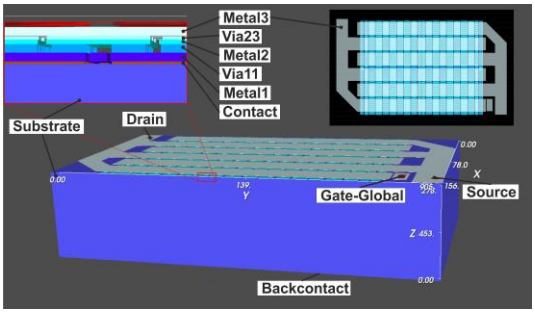

Fig. 1. Structure in a power transistor device [3].

II. Stochastic Forward Problem

The special construction of a power device, shown in Fig. 1, is considered here as a case study. The source and drain contacts are placed on the top of the design. It consists of several

thousands of parallel channel devices, where the current to drain and away from the sources of the individual channel is transported by complex series of metal stripes and via patterns. For the UQ analysis, we substitute some parameters $\boldsymbol{\xi}$ in a model (1) by independent random variables defined on some probabilistic space. Then, the current-flow pattern can be described by the coupled, random-dependent PDEs on $\Omega \subset \mathbf{R}^3$

$$\begin{cases} \nabla \cdot (\varepsilon \mathbf{E}) = \rho, \\ \nabla \cdot \mathbf{J}_{(n/p)} \mp q\partial_t (n/p) \mp qR(p,n) = \mathbf{0}, \\ \mathbf{J}_{(n/p)} = q \cdot (n/p) \cdot \mu_{(n/p)} \mathbf{E} \pm qD_{(n/p)} \nabla (n/p), \\ C_\upsilon \partial_t T = \nabla \cdot \lambda(T) \nabla T + \sigma \left\| \mathbf{E} \right\|^2, \end{cases} \tag{1}$$

endowed with suitable boundary and initials conditions. Here, ρ, ε and q denote the charge density, the permittivity and the elementary charge, respectively. $\mathbf{E}(\boldsymbol{x}, t, \boldsymbol{\xi})$ is the electric field. The concentration of holes and electrons is represented by n and p, while (n/p) describes compactly equations for electrons and holes. $D_{(n/p)}$, $\mu_{(n/p)}$, $\mathbf{J}_{(n/p)}$ $(\boldsymbol{x}, t, \boldsymbol{\xi})$ are the diffusion, mobility and current densities of electrons and holes. $T(\boldsymbol{x}, t, \boldsymbol{\xi})$, C_υ and $\lambda(T)$ denote the temperature, the heat capacitance and the thermal conductivity. The conductivity of k-th layer is defined as $\sigma = W_k \sigma_k$, where $\sigma_k = f(q, n, p, \mu_{(n/p)})$ and W_k is the layer size. The basic idea of using the SCM for the solution of a time-dependent random process (1) is to provide the solution of a deterministic problem at collocation points $\boldsymbol{\xi}^{(k)}$, $k = 0, ..., K$. This, in turn, also yields an approximation of statistical moments using the PC expansion [8], shown on Fig. 2 and 3.

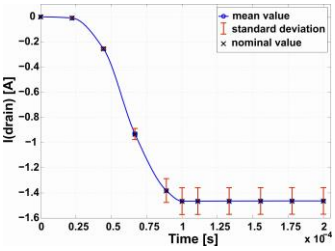

Fig. 2. UQ of I(drain) due to variations of the Metal3 thickness, modeled by a Gaussian distribution with 10% variation around a mean 1μm.

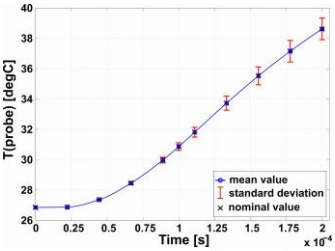

Fig. 3. UQ of T(probe) due to variations of the σ of the Metal3, modeled by a uniform distribution with 15% variation around a mean 20 MS/m.

III. Stochastic Optimization Problem

The problem of the shape optimization of the device layout corresponds to the minimization of a converted cost functional using the weighted aggregation method [4] in a mean sense $\mathbb{Q}$

$$\min_{\phi}^{\mathbb{Q}} [F] = w_1 \mathbb{Q}\left[I^{-1} \int_T \int_\Omega \mathbf{E}(\phi, \boldsymbol{\xi}) dx dt \right] + w_2 \mathbb{Q}\left[\sigma^{-1}(\phi, \boldsymbol{\xi}) \int_T \int_\Omega \left| \mathbf{J}(\phi, \boldsymbol{\xi}) \right|^2 dx dt \right] + \beta \int_\Gamma \left| \nabla \phi \right|^2 dx \tag{2}$$

where ϕ is a signed distance function. The fidelity term consists of two terms related to the output impedance and the dissipated electrical power. The Tikhonov regularization (last term) penalizes the oscillation of level sets with a smoothing effect, controlled by β. A priori information about objective functions is given by the prescribed weights w_1, w_2. To predict the sensitivity for the current source problem a Gâteaux differential can be used. Then, after formulating and solving the dual problem ($\mathbf{E}^*$), it is defined in the level set framework as

$$d_\phi F = \delta(\phi) \left[w_1 (\sigma_1 - \sigma_2) \int_T \int_\Gamma \mathbf{E} \cdot \mathbf{E}^* dx dt + w_2 \int_T \int_\Gamma \mathbf{J} \cdot \mathbf{E}^* dx dt \right] \tag{3}$$

with the Dirac function $\delta(\phi)$ and, e.g., σ represented by

$$\sigma(\phi, \boldsymbol{\xi}) = \sigma_1(\xi_1) H(\phi) + \sigma_2(\xi_1) \left[1 - H(\phi) \right] \tag{4}$$

With the smeared-out Heaviside function $H(\phi)$. For the voltage sensitivity problem, the Tellegen's theorem can be applied to incorporate results (3) into the optimization problem (2).

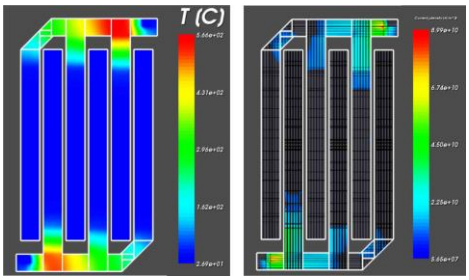

Fig. 4. Hot-spot phenomenon in the Metal3 layer for a case study [3]: temperature distribution (left), violations of current density (right).

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IV. References

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